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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/594,510	06/16/00	WOOD A	M4065.0184/P

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EXAMINER	
LUU, C	
ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 09/04/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

PTO-90C (Rev.11/00)

1- File Copy

Office Action Summary	Application No.	Applicant(s)	
	09/594,510	WOOD ET AL.	
	Examiner	Art Unit	
	Chuong A Luu	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 July 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18 and 35-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *19-23* is/are allowed.

6)☒ Claim(s) *1-18 and 35-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

Claims 24-34 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 4.

PRIOR ART REJECTIONS

Statutory Basis

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Th R jections

Claims 1, 5, 6, and 8-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Mizuno et al. (US 6,077,757)

Mizuno discloses a method of forming chip semiconductor devices by

(1) forming a layered assembly by attaching a wafer 14 to a dielectric layer (insulating substrate) 18; subsequently, testing semiconductor devices in said wafer 14 (see column 5, lines 1-12); and subsequently, dicing said layered assembly (see column 5, lines 52-67);

(5) wherein said step of forming said layered assembly includes the step of adhering said wafer to said dielectric layer (see column 5, line 19-35);

(6) further comprising the step of electrically connecting said semiconductor devices to ball grid arrays on said dielectric layer (see column 5, lines 36-53);

(8) wherein said connecting step comprises the step of connecting solder bumps on said wafer to circuit traces on said dielectric layer (see column 5, lines 36-53);

(9) wherein said dicing step is performed by a saw (see column 4, lines 17-24).

Claims 11-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Heo et al. (US 5,858,815)

(11) forming a layered assembly by attaching a semiconductor wafer and a metal (conductive) layer to a dielectric layer; connecting semiconductor devices in said semiconductor wafer to ball grid arrays on said dielectric layer;

subsequently, dicing said layered assembly;

(12) wherein said forming step comprises the step of adhering said wafer to said metal (conductive) layer;

(13) wherein said connecting step comprises the step of locating wire bonds in openings in said dielectric layer;

(14) further comprising the step of connecting said wire bonds to conductive traces on said dielectric layer;

(15) wherein said connecting step comprises the step of connecting solder bumps on said wafer to conductive traces on said dielectric layer;

(16) further comprising the step of connecting said traces to conductive vias extending through said dielectric layer;

(17) wherein said dicing step is performed by a saw;

(18) further comprising the step of testing said semiconductor devices through said ball grid arrays (see columns 4, 5, and 6, lines 36-67, lines 1-67, and lines 1-63, respectively).

Claims 2, 7, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mizuno et al. (US 6,077,757) in view of Heo et al. (US 5,858,815)

Mizuno teaches the above outlined features except for specific input/output devices, wire bonds or metal layer. However, Heo discloses a method for fabricating semiconductor package by

(2) further comprising the step of connecting said semiconductor devices to

input/output devices on the dielectric layer; **(3)** wherein said testing is conducted through said input/output devices (see column 8, lines 32-56); **(7)** wherein said connecting step comprises the step of locating wire bonds in openings through said dielectric layer (see columns 4, and 5, lines 49-57, and lines 1-17, respectively); **(10)** further comprising the step of providing a metal (conductive) layer in said layered assembly (see column 4, lines 58-67. Figure 13). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the teachings above to form a semiconductor device.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mizuno et al. (US 6,077,757) in view of Heo et al. (US 5,858,815), and further view of Lam (5,137,836)

Mizuno and Heo disclose everything above except for discarding one or more defective packages. However, Lam discloses a method of manufacturing a repairable multi-chip module by **(4)** further comprising the step of discarding one or more defective packages (see column 3, lines 1-60). It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings above to discarding one or more defective chip to fabricate a semiconductor device.

Claims 36, 37, and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mizuno et al. (US 6,077,757) in view of Kobayashi et al. (US 4,781,969)

Mizuno discloses a method of forming chip semiconductor devices by **(35)** connecting said semiconductor devices to respective ball grid arrays located on said flexible (insulating) substrate; testing said semiconductor devices through said ball grid arrays (see column 5, lines 1-12, and lines 52-67); **(37)** further comprising the step of singulating packages from said wafer and said substrate; **(38)** further comprising the step of segregating defective packages from other packages (see column 5, lines 1-12, and lines 52-67). Mizuno teaches the above outlined features but lacks a disclosure of specific use of a flexible substrate. However, Kobayashi discloses a printed circuit board with **(35).....** adhering said wafer to a flexible substrate (see column 1, lines 38-43). It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings of Mizuno and Kobayashi to employ a flexible substrate to serve the specific applicant to fabricate a semiconductor device.

Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mizuno et al. (US 6,077,757) in view of Kobayashi et al. (US 4,781,969), and further view of Lam (5,137,836)

Mizuno and Kobayashi diclose everything above except for identifying defective packages. Furthermore, Lam discloses a method of manufacturing a repairable multi-

chip module by **(4)** further comprising the step of discarding one or more defective packages (see column 3, lines 1-60). It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings above to discarding one or more defective chip to fabricate a semiconductor device.

Allowable Subject Matter

Claims 19-23 are allowed.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Mizuno et al., Lam, Kobayashi et al., and Heo et al. disclose a method of forming chip semiconductor devices.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A Luu whose telephone number is (703)305-0129. The examiner can normally be reached on M-F (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (703)308-1323. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Chuong Anh Luu
Assistant Examiner

CAL
August 23, 2001

MATTHEW SMITH
SUPERVISORY PATENT EXAMINER
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